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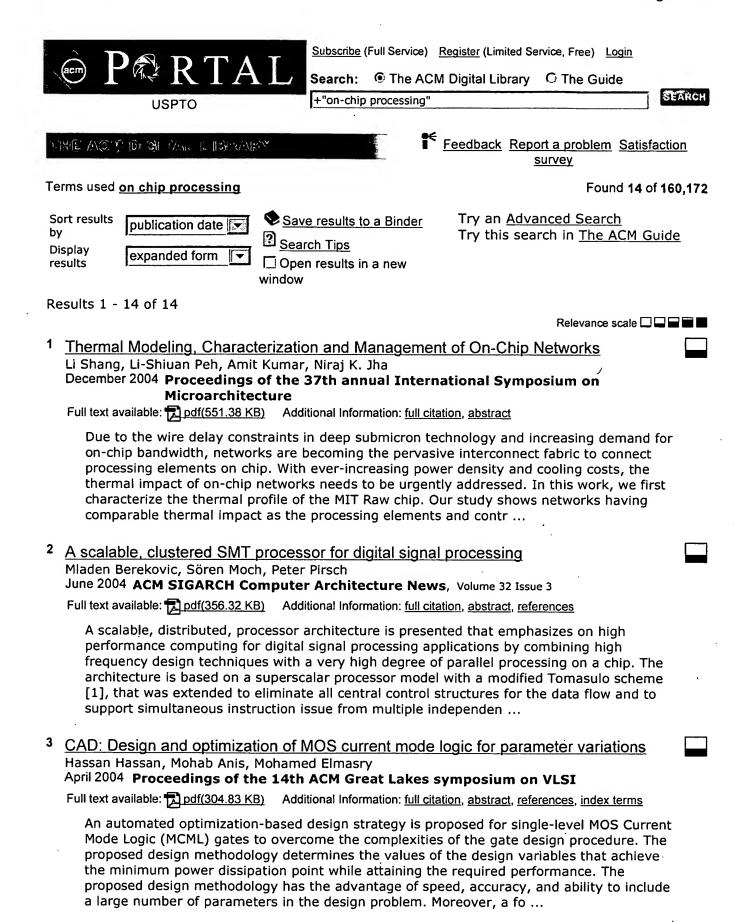
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4	Design styles (invited): Placement driven synthesis case studies on two sets of two chips: hierarchical and flat Peter J. Osler April 2004 Proceedings of the 2004 international symposium on Physical design
	Full text available: pdf(299.92 KB) Additional Information: full citation, abstract, index terms
	In this paper I describe two sets of two large ASIC chips that have recently been processed from netlist to final design by the Semi-Custom Design Team part of IBM's World-Wide Design Center. I address issues such as why the parts were selected for special handling, the issues with the designs that required custom engineering, and the special techniques used in placement driven synthesis that enabled successful completion of the designs.
	<b>Keywords</b> : application specific integrated circuit (ASIC), netlist, placement, register transfer level (RTL), static timing analysis (STA), synthesis
5	Hardware/Software Co-testing of Embedded Memories in Complex SOCs  Bai Hong Fang, Qiang Xu, Nicola Nicolici  November 2003 Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design
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	A novel approach for testing embedded memories in complexsystems-on-a-chip (SOCs) is presented. The proposedsolution aims to balance the usage of the existing on-chipresources and dedicated design for test (DFT) hardwaresuch that the functional power constraints are not exceededduring test while trading-off the testing time againstDFT area and performance overhead. The suitability ofsoftware-centric and hardware-centric approaches for embeddedmemory testing is examined and to combine the advanta
6	Design space exploration and architectural design of HW/SW systems: Hardware
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	The aggressive evolution of the semiconductor industry smaller process geometries, higher densities, and greater chip complexity has provided design engineers the means to create complex high-performance Systems-on-a-Chip (SoC) designs. Such SoC designs typically have more than one processor and huge memory, all on the same chip. Dealing with the global on- chip memory allocation/de-allocation in a dynamic yet deterministic way is an important issue for the upcoming billion transistor mu
	<b>Keywords</b> : Atalanta, SoCDMMU, System-on-a-Chip, dynamic memory management, embedded systems, real-time operating systems., real-time systems, two-level memory management
7	A reconfigurable multi-function computing cache architecture
-	Hue-Sung Kim, Arun K. Somani, Akhilesh Tyagi February 2000 Proceedings of the 2000 ACM/SIGDA eighth international symposium on Field programmable gate arrays

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A considerable portion of a chip is dedicated to a cache memory in a modern microprocessor chip. However, some applications may not actively need all the cache storage, especially the computing bandwidth limited applications. Instead, such applications may be able to use some additional computing resources. If the unused portion of the cache could serve these computation needs, the on-chip resources would be utilized more efficiently. This presents an opportunity to explore the reconfigurat ...

8 Converting a 64b PowerPC processor from CMOS bulk to SOI technology D. Allen, D. Behrends, B. Stanisic

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Full text available: pdf(90.91 KB)

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Microservers: a new memory semantics for massively parallel computing Jav B. Brockman, Peter M. Kogge, Thomas L. Sterling, Vincent W. Freeh, Shannon K. Kuntz May 1999 Proceedings of the 13th international conference on Supercomputing

Full text available: pdf(1.40 MB) Additional Information: full citation, references, citings, index terms

Keywords: massively parallel, microserver, processing-in-memory

10 Built-in self-test methodology for A/D converters

R. de Vries, T. Zwemstra, E. M. J. G. Bruls, P. P. L. Regtien

March 1997 Proceedings of the 1997 European conference on Design and Test

Full text available: pdf(632.08 KB) Publisher Site

Additional Information: full citation, abstract, citings

A (partial) Built-in Self-Test (BIST) methodology is proposed for analog to digital (A/D) converters. In this methodology the number of bits of the A/D converter that needs to be monitored externally in a test is reduced. This reduction depends, among other things, on the frequency of the applied test signal. At low test signal frequencies only the least significant bit (LSB) needs to be monitored and a "full" BIST becomes feasible. An analysis is made of the trade-off between the size of the on ...

**Keywords**: A/D converters, ADC testing, BIST methodology, analogue-digital conversion. built-in self-test, least significant bit, onchip test circuitry, test signal frequencies

11 Memory bandwidth limitations of future microprocessors

Doug Burger, James R. Goodman, Alain Kägi

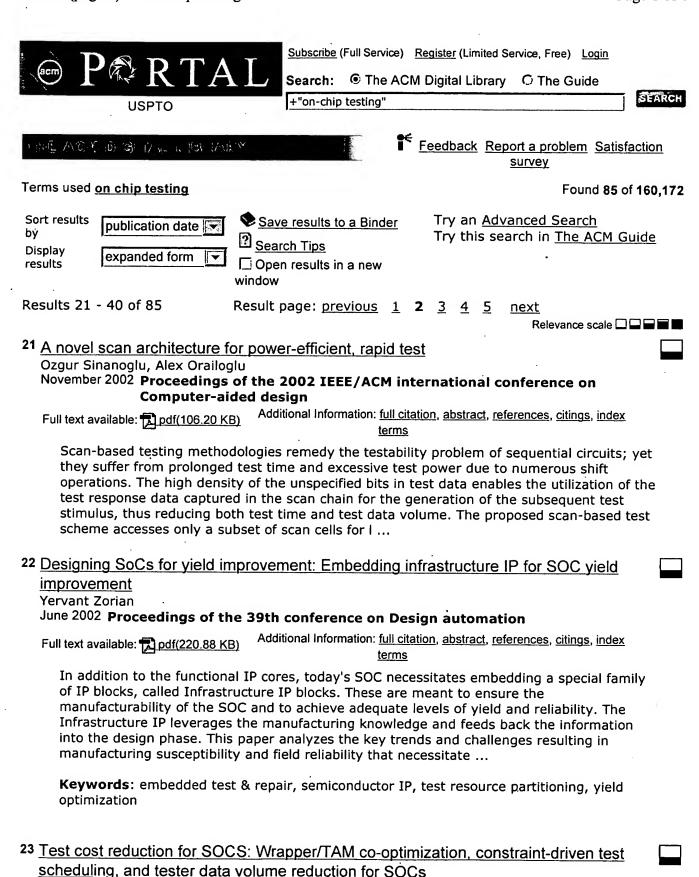
May 1996 ACM SIGARCH Computer Architecture News, Proceedings of the 23rd annual international symposium on Computer architecture, Volume 24 Issue 2

Full text available: pdf(1.60 MB)

Additional Information: full citation, abstract, references, citings, index terms

This paper makes the case that pin bandwidth will be a critical consideration for future microprocessors. We show that many of the techniques used to tolerate growing memory latencies do so at the expense of increased bandwidth requirements. Using a decomposition of execution time, we show that for modern processors that employ aggressive memory latency tolerance techniques, wasted cycles due to insufficient bandwidth generally exceed those due to raw memory latencies. Given the importance of ma ...

12 A laboratory for teaching parallel computing on parallel structures	_
Lan Jin, Lan Yang	
March 1995 ACM SIGCSE Bulletin , Proceedings of the twenty-sixth SIGCSE technical	
symposium on Computer science education, Volume 27 Issue 1  Full text available: Additional Information: full citation, abstract, references, citings, index	
Full text available: pdf(541.68 KB)  Additional information: tuli citation, abstract, references, citings, index terms	
For the effective use of a laboratory for teaching parallel processing, it is desirable to have parallel systems that can implement various parallel structures at hardware or software level. Such systems developed in our laboratories are described in this paper. They are a multi-computer with reconfiguration and the PVM (Parallel Virtual Machine) with structural implementation. The paper proposes a methodology and several classes of problems for teaching message-passing programming on paral	
13 A fast and flexible performance simulator for micro-architecture trade-off analysis on	
UltraSPARC-I	
Marc Tremblay, Guillermo Maturana, Atsushi Inoue, Les Kohn January 1995 <b>Proceedings of the 32nd ACM/IEEE conference on Design automation</b>	
Full text available: pdf(70.91 KB) Additional Information: full citation, references, citings, index terms	
14 Simulation of a pyramid processor	
Duane R. Ball, Gerard C. Blais, David Schaefer, Gregory Wilcox, R. Neil Wagoner December 1985 <b>Proceedings of the 17th conference on Winter simulation</b>	
Full text available: pdf(434.39 KB) Additional Information: full citation, abstract, references	
This paper describes a simulation model of the MPP Pyramid [1] that has been constructed at the George Mason University. This model has been designed to facilitate experiments in processor control and in instruction set design.	
Results 1 - 14 of 14	
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Additional Information: full citation, abstract, references, citings, index

<u>terms</u>

Vikram Iyengar, Krishnendu Chakrabarty, Erik Jan Marinissen

Full text available: pdf(168.08 KB)

June 2002 Proceedings of the 39th conference on Design automation

This paper describes an integrated framework for plug-and-play SOC test automation. This framework is based on a new approach for wrapper/TAM co optimization based on rectangle packing. We first tailor TAM widths to each core's test data needs. We then use rectangle packing to develop an integrated scheduling algorithm that incorporates precedence and power constraints in the test schedule, while allowing the SOC integrator to designate a group of tests as preemptable. Finally, we study the rela ...

24	New test methods targeting non-classical faults: Embedded software-based self-testing	-
	or SoC design	,

A. Krstic, W. C. Lai, K. T. Cheng, L. Chen, S. Dey

June 2002 Proceedings of the 39th conference on Design automation

Full text available: pdf(324.94 KB) Additional Information: full citation, abstract, references, index terms

At-speed testing of high-speed circuits is becoming increasingly difficult with external testers due to the growing gap between design and tester performance, growing cost of high-performance testers and increasing yield loss caused by inherent tester inaccuracy. Therefore, empowering the chip to test itself seems like a natural solution. Hardware-based self-testing techniques have limitations due to performance and area overhead and problems caused by the application of non-functional patterns. ...

Keywords: SoC test, VLSI test, functional test, microprocessor test

### 25 Testing and Fault-Tolerance: Minimizing concurrent test time in SoC's by balancing resource usage

Dan Zhao, Shambhu Upadhyaya, Martin Margala

April 2002 Proceedings of the 12th ACM Great Lakes symposium on VLSI

Additional Information: full citation, abstract, references, index terms Full text available: pdf(87.90 KB)

We present a novel test scheduling algorithm for embedded core-based SoC's. Given a system integrated with a set of cores and a set of test resources, we select a test for each core from a set of alternative test sets, and schedule it in a way that evenly balances the resource usage, and ultimately reduce the test application time. Furthermore, we propose a novel approach that groups the cores and assigns higher priority to those with smaller number of alternate test sets. In addition, we also e ...

**Keywords**: resource balancing, system-on-a-chip test scheduling, test sets selection

## 26 Efficient Wrapper/TAM Co-Optimization for Large SOCs

V. Iyengar, K. Chakrabarty, E. Marinissen

March 2002 Proceedings of the conference on Design, automation and test in Europe

Full text available: pdf(225.35 KB)

Additional Information: full citation, abstract, citings

Core test wrappers and test access mechanisms (TAMs) are important components of a system-on-chip (SOC) test architecture. Wrapper/TAM co-optimization is necessary to minimize the SOC testingtime. Most prior research in wrapper/TAM design has addressedwrapper design and TAM optimization as separate problems, therebyleading to results that are sub-optimal. We present a fast heuristictechnique for wrapper/TAM cooptimization, and demonstrate its scalability for several industrial SOCs. This extends r ...

## <sup>27</sup> Effective Software Self-Test Methodology for Processor Cores

N. Kranitis, A. Paschalis, D. Gizopoulos, Y. Zorian

March 2002 Proceedings of the conference on Design, automation and test in Europe

	Full text available: pdf(284.27 KB) Additional Information: full citation, abstract  Publisher Site	
	Software self-testing for embedded processor coresbased on their instruction set, is a top of increasing interest since it provides an excellent test resourcepartitioning technique for sharing the testing task of complex Systems-on-Chip (SoC) between slow, inexpensive testers and embedded code stored in memorycores of the SoC. We introduce an efficient methodology for processor cores self-testing which requires knowledge of their instruction set and Register Transfer (RT) leveldescription. Compared	
28	Improving Compression Ratio, Area Overhead, and Test Application Time for System on-a-Chip Test Data Compression/Decompression P. Gonciari, B. Al-Hashimi, N. Nicolici March 2002 Proceedings of the conference on Design, automation and test in Europe	
	Full text available: pdf(162.69 KB) Additional Information: full citation, abstract, citings Publisher Site	
	This paper proposes a new test data compression/decompression method for systems-on chip. Themethod is based on analyzing the factors that influencetest parameters: compression ratio, area overhead and testapplication time. To improve compression ratio the newmethod is based on a Variable-length Input Huffman Coding(VIHC), which fully exploits the type and length of the patterns, as well as a novel mapping and reordering algorithmproposed in a pre-processing step. The new VIHC algorithmis comb	
29	Test Planning and Design Space Exploration in a Core-Based Environment	
	E. Cota, L. Carro, M. Lubaszewski, A. Orailoglu March 2002 <b>Proceedings of the conference on Design, automation and test in Europe</b>	1
	Full text available: pdf(133.63 KB) Additional Information: full citation, abstract, citings	
	This paper proposes a comprehensive model for testplanning in a core-based environment. The main contribution of this work is the use of several types of TAMs and the consideration of different optimization factors (area, pinsand test time) during the global TAM and test schedule definition. This expansion of concerns makes possible an efficientyet fine-grained search in the huge design space of a reuse-based environment. Experimental results clearly show the variety of trade-offs that can be explore	n
30	Cellular and Cryptographic Applications: FPGA implementation of neighborhood-of-	
	four cellular automata random number generators  Barry Shackleford, Motoo Tanaka, Richard J. Carter, Greg Snider  February 2002 Proceedings of the 2002 ACM/SIGDA tenth international symposium of	on

Field-programmable gate arrays

Full text available: pdf(565.95 KB) Additional Information: full citation, abstract, references

Random number generators (RNGs) based upon neighborhood-of-four cellular automata (CA) with asymmetrical, non-local connections are explored. A number of RNGs that pass Marsaglia's rigorous Diehard suite of random number tests have been discovered. A neighborhood size of four allows a single CA cell to be implemented with a four-input lookup table and a one-bit register which are common building blocks in popular field programmable gate arrays (FPGAs). The investigated networks all had periodic ...

Keywords: FPGA, cellular automata, random number generator

Patterns for Testing Embedded Core Based System Using Test

#### Access Mechanism (TAM) Switch

Subhayu Basu, Debdeep Mukhopadhay, Dipanwita Roychoudhury, Indranil Sengupta, Sudipta Bhawmik

January 2002 Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design



Additional Information: full citation, abstract

In the present paper a new algorithm for reformatting the test vector of System On Chip (SOC) with Test Access Mechanism (TAM) has been proposed. Exhaustive experimentation has been done by employing random reformatted test vectors to a variety of SOCs. constructed with the ISCAS sequential benchmark circuits. For a limited number of input pins, which has been provided for testing the SOC, the proposed algorithm reduces drastically the test-time as well as the hardware.

Keywords: Test Access Mechanism, Data acyclic graph, Test patterns, Test time, Systemon-Chip

### 32 Design of An On-Chip Test Pattern Generator Without Prohibited Pattern Set (PPS)



Niloy Ganguly, Biplab K. Sikdar, P P. al Chaudhuri

January 2002 Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design



Additional Information: full citation, abstract

This paper reports the design of a T est P attern Generator (TPG) for V LSI circuits. The onchip TPG is so designed that it generates test patterns while avoiding generation of a given Prohibited Pattern Set (PPS). The design ensures desired pseudo-random quality of the test patterns generated. The experimental results confirm high quality of randomness while ensuring fault coverage close to the figures achieved with a typical Pseudo Random Pattern Generator (PRPG) designed around maximal length ...

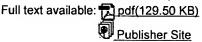
# 33 A Partitioning and Storage Based Built-In Test Pattern Generation Method for Scan



Circuits

Irith Pomeranz, Sudhakar M. Reddy

January 2002 Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design



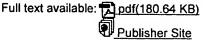
Additional Information: full citation, abstract

We describe a built-in test pattern generation method for scan circuits. The method is based on partitioning and storage of test sets. Under this method, a precomputed test set is partitioned into several sets containing values of different primary inputs or state variables. The on-chip test set is obtained by implementing the Cartesian product of the various sets. The sets are reduced as much as possible before they are stored on-chip in order to reduce the storage requirements and the test applicat ...

#### 34 On Test Scheduling for Core-Based SOCs

Sandeep Koranne

January 2002 Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design



Additional Information: full citation, abstract, citings

We present a mathematical model for the problem of scheduling tests for core-based

system-on-chip (SOC) VLSI designs. Given a set of tests for each core in the SOC and a set of test resources (e.g., test access mechanisms (TAM)), we determine the test plan for the application of the tests to the SOC. Test planning in this paper refers to the combined activities of test access architecture partitioning and test scheduling. These activities must be performed in conjunction as the choice of the tes ...

35	Session 9A:	<u>System</u>	<u>level test</u>	and	<u>reliability:</u>	<u>The</u>	design	and	optimizati	on o	f SOC	C test
	solutions						_					

Erik Larsson, Zebo Peng, Gunnar Carlsson

November 2001 Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design

Full text available: pdf(182.66 KB) Additional Information: full citation, abstract, references, index terms

We propose an integrated technique for extensive optimization of the final test solution for System-on-Chip using Simulated Annealing. The produced results from the technique are a minimized test schedule fulfilling test conflicts under test power constraints and an optimized design of the test access mechanism. We have implemented the proposed algorithm and performed experiments with several benchmarks and industrial designs to show the usefulness and efficiency of our technique.

#### 36 Von Neumann hybrid cellular automata for generating deterministic test sequences D. Kagaris, S. Tragoudas

July 2001 ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 6 Issue 3

Full text available: pdf(143.85 KB) Additional Information: full citation, abstract, references, index terms

We propose an on-chip test pattern generator that uses an one-dimensional cellular automaton (CA) to generate either a precomputed sequence of test patterns or pairs of test patterns for path delay faults. To our knowledge, this is the first approach that guarantees successful on-chip generation of a given test pattern sequence (or a given test set for path delay faults) using a finite number of CA cells. Given a pair of columns (Cu. C Keywords: built-in self-test (BIST), cellular automata, test pattern generation

#### 37 Intrinsic response for analog module testing using an analog testability bus Chauchin Su, Yue-Tsang Chen, Shyh-Jye Jou

April 2001 ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 6 Issue 2

Full text available: pdf(277.66 KB) Additional Information: full citation, abstract, references, index terms

A parasitic effect removal methodology is proposed to handle the large parasitic effects in analog testability buses. The removal is done by an on-chip test generation technique and an intrinsic response extraction algorithm. On-chip test generation creates test signals onchip to avoid the parasitic effects of the test application bus. The intrinsic response extraction cross-checks and cancels the parasitic effects of both test application and response observation paths. The tests using bo ...

Keywords: analog testability bus, analog testing, boundary scan, design for testability, intrinsic response

## <sup>38</sup> An integrated system-on-chip test framework

E. Larsson, Z. Peng

March 2001 Proceedings of the conference on Design, automation and test in Europe

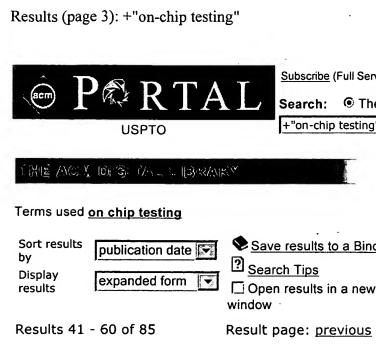
Full text available: pdf(139.63 KB) Additional Information: full citation, references, citings, index terms

39	Embedded tutorial: TRP: integrating embedded test and ATE  Y. Zorian, P. Prinetto, J. Teixeira, I. Teixeira, C. Pereira, O. Dias, J. Semiao, P. Muhmenthaler, W. Radermacher March 2001 Proceedings of the conference on Design, automation and test in Europe Full text available: pdf(67.84 KB)  Additional Information: full citation, references, index terms
	A TOTAL CONTROL OF THE PARTY OF
	·
40	Synthesis of single-output space compactors with application to scan-based IP cores  Bhargab B. Bhattacharya, Alexej Dmitriev, Michael Gössel, Krishendu Chakrabarty  January 2001 Proceedings of the 2001 conference on Asia South Pacific design  automation  Full text available: pdf(287.16 KB) Additional Information: full citation, abstract, references, index terms
	This paper addresses the problem of space compaction of test responses of combinational and scan-based sequential circuits. It is shown that given a precomputed test set T, the test responses at the functional outputs of the given circuit-under-test (CUT) can be compacted to a single periodic output, with guaranteed zero-aliasing. The method is independent of the fault model and the structure of the CUT, and uses only the knowledge of the test set T and the corresponding fault-free response

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41 Cellular automata as a built in self test structure

Biplab K. Sikdar, Debesh K. Das, Vamsi Boppana, Cliff Yang, Sobhan Mukherjee, P. Pal Chaudhuri

January 2001 Proceedings of the 2001 conference on Asia South Pacific design automation

Full text available: pdf(296.56 KB) Additional Information: full citation, abstract, references, index terms

This paper presents an efficient BIST solution for VLSI circuit testing based on GF(2p) CA (Cellular automata on an extended Galois Field). The novel architecture of GF(2p)) CA permits the BIST structure to be highly customized to the circuit under test (CUT). A methodology has been proposed to optimize the design of GF(2p) CA structure to maximize the fault coverage in a given CUT. In addition, an innovative scheme based on logic folding is presented to reduce the BIST overhead and make it ...

42 Optimal test access architectures for system-on-a-chip

Krishnendu Chakrabarty

January 2001 ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 6 Issue 1

Additional Information: full citation, abstract, references, citings, index Full text available: pdf(197.95 KB) terms

Test access is a major problem for core-based system-on-a-chip (SOC) designs. Since embedded cores in an SOC are not directly accessible via chip inputs and outputs, special access mechanisms are required to test them at the system level. An efficient test access architecture should also reduce test cost by minimizing test application time. We address several issues related to the design of optimal test access architectures that minimize testing time., including the assignment of cores to t ...

43 Session 8D: embedded tutorial: Test of future system-on-chips

Yervant Zorian, Sujit Dey, Michael J. Rodgers

November 2000 Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design

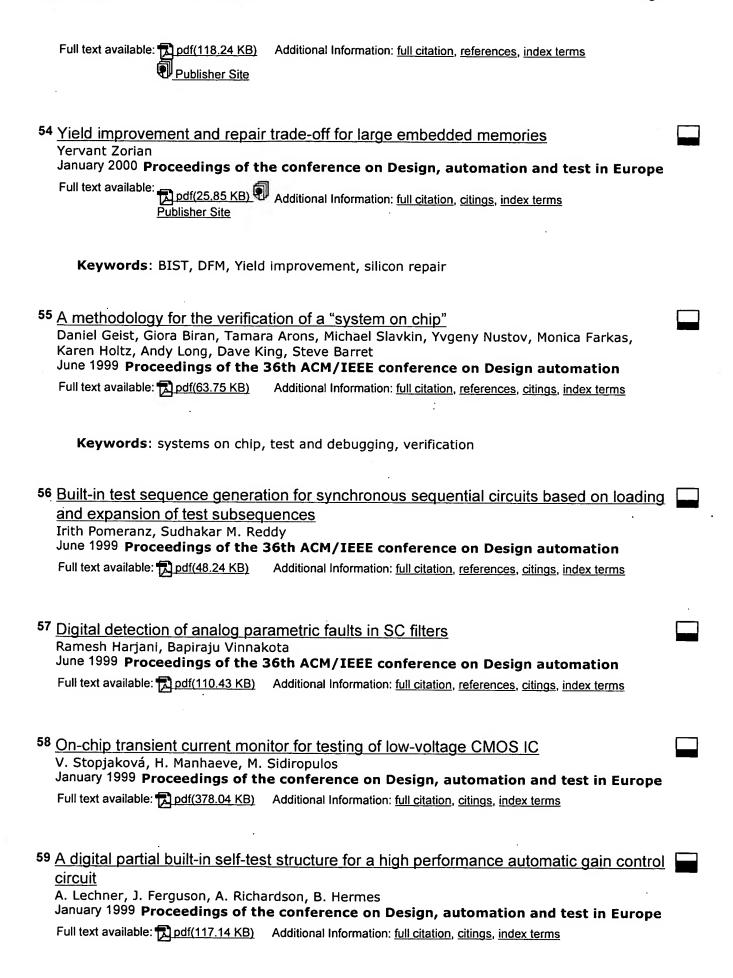
Full text available: pdf(140.88 KB) Additional Information: full citation, abstract, references, citings

Spurred by technology leading to the availability of millions of gates per chip, system-level integration is evolving as a new paradigm, allowing entire systems to be built on a single chip. Being able to rapidly develop, manufacture, test, debug and verify complex SOCs is crucial for the continued success of the electronics industry. This growth is expected to continue full force at least for the next decade, while making possible the production of

multimillion transistor chips. However, to mak ...

44	Session 9D: new approaches to at-speed BIST and diagnosis: Diagnosis of interconnect faults in cluster-based FPGA architectures  Ian Harris, Russell Tessier	
	November 2000 Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design	
	Full text available: pdf(60.64 KB) Additional Information: full citation, abstract, references, citings	
	Fault diagnosis has particular importance in the context of field programmable gate arrays (FPGAs) because faults can be avoided by reconfiguration at almost no real cost. Cluster-based FPGA architectures, in which several logic blocks are grouped together into a coarse-grained logic block, are rapidly becoming the architecture of choice for major FPGA manufacturers. The high density interconnect found within clusters greatly complicates the problem of FPGA diagnosis. We propose a technique for	
45	Verification of configurable processor cores	
	Marinés Puig-Medina, Gülbin Ezer, Pavlos Konas June 2000 Proceedings of the 37th conference on Design automation	
,	Full text available: pdf(79.05 KB)  Additional Information: full citation, abstract, references, citings	
	This paper presents a verification methodology for configurable processor cores. The simulation-based approach uses directed diagnostics and pseudo-random program generators both of which are tailored to specific processor instances. A configurable and extensible test-bench serves as the framework for the verification process and offers components necessary for the complete SOC verification. Coverage analysis provides an evaluation of how well a specific design has been exercised, of the br	
	<b>Keywords</b> : co-simulation, configurable processor cores, coverage analysis, design verification, system-on-chip, test generation	
46	Design of system-on-a-chip test access architectures under place-and-route and power	·
	<u>constraints</u>	
	Krishnendu Chakrabarty June 2000 Proceedings of the 37th conference on Design automation	
	Full text available: pdf(108.28 KB)  Additional Information: full citation, abstract, references, citings, index terms	
	Test access is a difficult problem encountered in the testing of core-based system-on-a-chip (SOC) designs. Since embedded cores in an SOC are not directly accessible via chip inputs and outputs, special access mechanisms are required to test them at the system level. We propose test access architectures based on integer linear programming (ILP) that incorporate place-and-route constraints arising from the functional interconnections between cores, as well as system-level constraint	
47	Embedded hardware and software self-testing methodologies for processor cores	
	Li Chen, Sujit Dey, Pablo Sanchez, Krishna Sekar, Ying Cheng June 2000 <b>Proceedings of the 37th conference on Design automation</b>	
	Full text available: pdf(103.87 KB)  Additional Information: full citation, abstract, references, citings, index terms	
	At-speed testing of GHz processors using external testers may not be technically and economically feasible. Hence, there is an emerging need for low-cost, high-quality self-test methodologies, which can be used by processors to test themselves at-speed. Currently, Built-In Self-Test (BIST) is the primary self-test methodology available and is widely used	

for testing embedded memory cores. In this paper, we report our experiences in applying a commercial BIST methodology to two processor cor ... 48 Improved fault diagnosis in scan-based BIST via superposition Ismet Bayraktaroglu, Alex Orailoğlu June 2000 Proceedings of the 37th conference on Design automation Additional Information: full citation, abstract, references, citings, index Full text available: pdf(80.86 KB) terms An improved approach for diagnosis of scan-based BIST designs is proposed. The enhancement in diagnosis is achieved by utilizing the superposition principle. Scan cells are partitioned pseudorandomly for observation and the ones provably fault free are removed from the potentially faulty list. Diagnostic resolution is improved by a novel application of the superposition principle, resulting in significant reductions in diagnosis time. 49 Self-test methodology for at-speed test of crosstalk in chip interconnects Xiaoliang Bai, Sujit Dey, Janusz Rajski June 2000 Proceedings of the 37th conference on Design automation Additional Information: full citation, abstract, references, citings, index Full text available: pdf(113.37 KB) The effect of crosstalk errors is most significant in high-performance circuits, mandating atspeed testing for crosstalk defects. This paper describes a self-test methodology that we have developed to enable on-chip at-speed testing of crosstalk defects in System-on-Chip interconnects. The self-test methodology is based on the Maximal Aggressor Fault Model [13], that enables testing of the interconnect with a linear number of test patterns. To enable self-testing of the interconnects, we h ... 50 A sigma-delta modulation based BIST scheme for mixed-signal circuits Jiun-Lang Huang, Kwang-Ting Cheng January 2000 Proceedings of the 2000 conference on Asia South Pacific design automation Full text available: pdf(117.31 KB) Additional Information: full citation, references, citings 51 A BIST scheme for on-chip ADC and DAC testing Jiun-Lang Huang, Chee-Kian Ong, Kwang-Ting Cheng January 2000 Proceedings of the conference on Design, automation and test in Europe Full text available: pdf(114.67 KB) Additional Information: full citation, references, citings, index terms Publisher Site 52 Built-in generation of weighted test sequences for synchronous sequential circuits Irith Pomeranz, Sudhakar M. Reddy January 2000 Proceedings of the conference on Design, automation and test in Europe Full text available: pdf(66.38 KB) Additional Information: full citation, references, index terms **Publisher Site** 53 An on chip ADC test structure Yun-Che Wen, Kuen-Jong Lee January 2000 Proceedings of the conference on Design, automation and test in Europe



60 Design for testability method for CML digital circuits

Bernard Antaki, Yvon Savaria, Saman M. I. Adham, Nanhan Xiong

January 1999 Proceedings of the conference on Design, automation and test in Europe Full text available: pdf(218.86 KB) Additional Information: full citation, index terms

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